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A First Level Tracking Trigger for the Upgraded DØ Detector

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Abstract

A fast tracking trigger system based on a new scintillating fiber tracker is being built for the upgraded DØ detector for the Collider Run II at Fermilab. This fiber tracker trigger provides a first level hardware trigger, supplies track seeds for the first level muon trigger and for the second level trigger. The physics requirements and the corresponding algorithms for the hardware trigger will be described. Particularly, PLD (Programmable Logical Device) chips are used to implement our trigger algorithms to achieve pattern recognition from scintillating fiber hits and to format that information for delivery to other trigger systems. Detector trigger efficiency studies will also be presented.

I. INTRODUCTION

For the Collider Run II at Fermilab, the upgraded DØ detector will have a new tracking system using scintillating fibers, called the Central Fiber Tracker (CFT). The CFT is an essential part of our Level 1 and Level 2 trigger systems and many other triggers depend on it. [1]

There are three levels of trigger hierarchy in DØ. Level 1 (L1) consists of custom hardware based triggers which search for patterns consistent with muons, electrons and jets. Level 2 (L2) uses DEC Alpha processors and DSP's (Digital Signal Processors) to combine L1 objects and additional hit information into muons, electrons and jets. Level 3 (L3) is a computer farm which uses offline algorithms for particle identification. The maximum trigger rates for events passing L1, L2 and L3 are about 10kHz, 1kHz and 10 Hz respectively.

The CFT consists of 32 concentric barrel-shaped layers of scintillating fibers that are arranged in 16 "doublet" layers. Half of the doublet layers have fibers parallel to the z-axis (called axial layers) and the other half are at an angle (stereo layers). Only the 8 axial doublet layers are used in the CFT trigger. The fiber diameter is 835 μm. The radii of the CFT layers range from about 20 cm to 52 cm and it offers full coverage down to about 22° in polar angle. A 2 Tesla solenoid magnet around the CFT provides the field which bends the charged tracks in the radial plane of the CFT.

The goal for the Level 1 CFT trigger is to provide triggers for all charged particles with transverse momenta as low as 1.5 GeV at the highest possible efficiency. The beam crossing rate is about 7.6 MHz and the Level 1 trigger is designed to accept a new event every 132 ns. The L1 trigger system has to accommodate a peak luminosity of $2x10^{32}/cm^2/s$ such that each beam crossing may give rise to more than a hundred charged tracks. Since the L1 muon trigger needs to have CFT tracks as seeds, a list of track information must be passed to the L1 muon trigger system within about 800 ns after beam crossing. A global L1 trigger decision needs to reach the trigger manager within 3.6 μs after beam crossing. Sufficient buffering is employed so that the L1 trigger system has less than 5% deadtime.

II. CFT FRONT END BOARD

A. CFT Front End Board Overview

A hardware implementation of the Level 1 CFT trigger system has been developed. Most of the functionality and components are situated directly on the detector, in the Front End (FE) Boards. The CFT is divided equally into 80 sectors or wedges in the rϕ plane, one sector (subtending 4.5°) per FE board. There are 480 fibers on the axial layers in each sector of the CFT.

The FE boards are mounted on the VLPC (Visible Light Photon Counter) cassettes which are in turn inserted into the top of two VLPC cryostats. VLPC's are used to convert the light produced in the scintillating fibers of the CFT due to the passage of charged tracks. [2] The principal functions of the FE board are VLPC signal processing, producing a fast trigger signal, finding the track and reporting the trigger information. Each FE board has 8 Multiple-chip-modules (MCM's), each of which contains one SVX (Silicon Vertex) chip and four SIFT (**S**c**I**ntillating **F**iber **T**racking) chips. [3]

The expected average signal level from the VLPC is about 30000 electrons per photoelectron and the longest charge collection time is about 70ns. The number of photoelectrons in a single fiber for a single track is between 10 and 40. The fiber signals from the VLPC's need to be digitized and discriminated. The ADC is the SVX IIe chip which was originally developed for the silicon detector. However, in order to meet the timing and charge integration requirements, the custom chip (called SIFT) has been designed as a front end to the SVX chip with a charge acquisition time of 70 ns and a selectable discriminator range and gain. The output of the discriminator stage is latched to an output driver and remains high for about 100 ns. The signal is TTL, which is suitable for driving the trigger logic we use.

At the lowest P_T threshold envisioned (1.5 GeV), all tracks which cross the outermost CFT layer (H layer) of a 4.5° sector are either completely contained in the sector, or partly in the sector and partly in an adjacent sector. To form a seamless trigger for all tracks which intercept the H layer, hit information from the two neighbor sectors are imported.

When the logic signal for each of the home sector fibers exits the MCM, it is latched into a PLD (Programmable Logical Device). Latching removes the time scatter of the signals due to different polar angles of the tracks, light path length differences and other sources. This latching PLD then distributes the signals from the home sector to the track finding logic on the home FE board and to the logic on each of the two neighbor sectors.

Each FE board has a number of PLD's responsible for the track finding logic. Each PLD receives fiber signals from hundreds of fibers in the home sector as well as from its neighbors. A set of predefined candidate trajectories for different P_T ranges are downloaded into each PLD. Each PLD executes the pattern recognition algorithm to find track candidates and reports the number of track candidates found and the coded position and momentum indices for the first six tracks in each of four P_T threshold bins.

PLD's are used in the CFT trigger logic so that one can quite flexibly program (or reprogram) the trigger logic in these devices when they are in place on the detector. Standard VHDL (VHSIC Hardware Description Language) code is used for this task and a trigger test board applying the baseline tracking algorithm has been fabricated and tested. [4]

B. Doublet Finding

Each of the 8 doublet layers in the CFT is made up of two single layers. One of the layers is staggered by half a fiber spacing relative to the other so that there are no gaps. In principle, all tracks pass through a fiber in the inner, the outer or both layers.

The first part of finding a track is to form bins in each doublet layer by combining individual fiber hits in the inner and outer singlet layers. A doublet bin is a logical combination of inner and outer fibers and it is formed in such a way that the doublet bins do not overlap and each of them is one fiber wide. The doublet bin, DOUBLET[j] is defined logically as follows:

$$\begin{aligned} \text{DOUBLET[j]} = \{ & \text{NOT(OUTER[j]) AND INNER[j]} \} \\ & \text{OR OUTER[j+1]}, \end{aligned} \quad (1)$$

where OUTER[k] and INNER[k] correspond to the outer and inner singlet fiber indices respectively. Figure 1 illustrates the above definition.

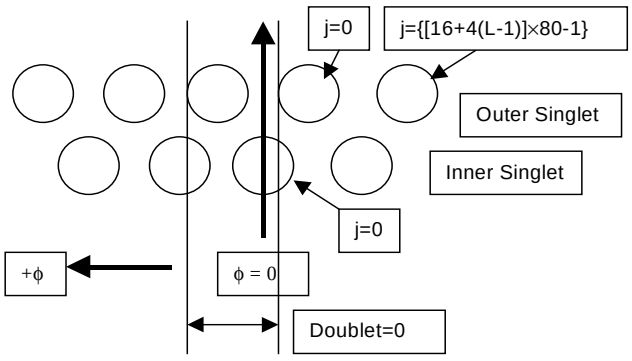

Figure 1 This view shows the numbering system for the singlet fibers and the doublet bins. Note that the inner singlet fiber j=0 is centered at ϕ=0, but the outer j=0 fiber is at -ϕ. Note also that doublet bin 0 starts at a -ϕ value. "L" stands for the Lth doublet layer in the CFT.

The "OR" combines the inner and outer layers. The "AND" with the "NOT" makes the bins non-overlapping. Exactly the above equation and the meaning of the indices is used in the FE Trigger software, the Monte Carlo simulation software, and the online and offline analysis software.

C. Track Finding

The goal of the track finder is to achieve the highest efficiency for finding the real tracks while maintaining the largest possible rejection factor against fake tracks. For the configuration of the CFT, the greatest rejection is achieved in the trigger if a hit is required on all of the eight layers of the tracker and the trajectory width at each layer is one fiber pitch wide, about 1mm. Wider roads result in too many extra fake tracks. Narrower roads may lose real tracks due to multiple scattering and other radiation effects.

The baseline design therefore requires a hit in each of the 8 layers and the 8 doublet hits (bins) are then combined to form a track. A trigger requiring 8 hits out of 8 layers can be used because the efficiency for each doublet layer is over 99.5%. Nevertheless, the scintillating fiber efficiency may deteriorate during the experiment run due to aging and radiation damage especially if we see high luminosity for much of the run. If it becomes necessary, we may require only 7 hits out of 8 layers for tracks in the highest P_T range. There would be too many candidate trajectories to deal with if we also allowed 7 out of 8 for tracks with lower P_T.

Section III describes in detail how we find the candidate trajectories (called equations) and how the tracking logic is implemented in the PLD's.

D. PLD Download and Test

Each of the large PLD's responsible for the tracking logic requires more than a hundred kilobits of information for its programming, which would be lost on any power interruption. A download system is located on each FE board consisting of non-volatile memory (an AMD Flash RAM), which stores a copy of the programs for all PLD chips on the board, and a download controller that is a non-volatile PLD[1]. Upon power up or reset, the download controller resets itself and then downloads all the PLD's from the non-volatile memory.

During the design, we rely on vendor[2] software to simulate our trigger logic with the types of the PLD's that we intend to use. We have also set up a trigger test board which has the necessary PLD's installed to test the trigger algorithm. Both software simulation and hardware test indicate that the tracking logic can be accomplished well within 132 ns which is the timing constraint that we have. Perhaps more importantly, the trigger timing quoted in the simulation agrees well with the timing measurements made with the trigger test board. Our setup time requirement for latching in the fiber inputs in the PLD's is about 13 ns and this is also met. In addition the outputs from the tracking logic also agree with what we expect.

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[1] This kind of non-volatile PLD (usually referred to as CPLD) does not have enough logic resources for the intensive tracking logic.

[2] Two main vendors have been considered, namely, "Altera" and "Xilinx".

III. TRACKING ALGORITHM

Since several other trigger components in the experiment depend on the L1 CFT trigger, we have done a detailed study of the tracking algorithm to make sure that the L1 CFT trigger track output meets all the physics requirements. Monte Carlo simulations of the upgraded DØ detector have been used to investigate the outcome of different methods. As far as the CFT FE board is concerned, the Monte Carlo simulation shows that we can limit ourselves to allowing only 2 tracks per doublet bin in the anchor layer (H layer) and only 6 tracks in each of the 4 P_T thresholds (i.e. 24 tracks) in each sector virtually without losing any track efficiency. This has been incorporated in the tracking algorithm as described below.

A. Equation Generation

Before we can calibrate the CFT with the real tracking data after the experiment starts to run, we have to use our best guess to find a set of equations for the trigger logic. The basic algorithm to generate the equations analytically is given as follows. A special particle tracing Monte Carlo simulation has also been used to cross check the results. For convenience, from now on, we consider doublet bins as doublet fibers. Two doublet layers are used as starting reference fibers, the innermost layer and the anchor layer as shown in Figure 2. Though we use the outermost layer as the anchor layer, for the purpose of generality any layer (except the innermost one) can be the anchor layer in the following explanation.

The basic equation for a charged particle moving transverse to a magnetic field is

$$\phi_O = \phi - \frac{kr}{P_T} \qquad (2)$$

where ϕ_o is the tangent angle of the track at the origin (radius r=0), ϕ is the tangent angle at radius r, k is a constant and P_T is the particle momentum transverse to the magnetic field. Given two fibers at different radii, there are a minimum and a maximum P_T that can intersect these two fibers (see Figure 2). These can be found by solving equation (2) for $\phi_o$and P_T given r_1, r_2, ϕ_1, ϕ_2 (2 equations and 2 unknowns).

Using the anchor layer, the edges of each innermost layer fiber define a minimum P_T track and a maximum P_T track. This assumes that all tracks pass through the origin. Using the trajectories of these two tracks, we can find all the fibers in the layers in between that lie within this P_T. That is, given P_T, ϕ_o, and r, we solve for the minimum and maximum ϕ at each layer and then select all the fibers that are in this ϕ range. Next, we choose one fiber from each layer from this list of fibers. The minimum and maximum P_T of this set of 8 fibers will be determined by two of these fibers but we do not know which two. So, we compute the minimum and maximum P_T for all possible pairs of fibers. This is 7×8 or 56 pairs for the 8 layers case since the self term (same fiber) is not possible. Not all of these P_T pairs will pass through all 8 fiber layers. To find the ones that do, we calculate ϕ_o from equation (2) for all 8 layers for both the minimum and maximum P_T. From geometry, we see that the maximum of the 8 ϕ_o's calculated from the minimum P_T trajectories must be less than the minimum of the 8 ϕ_o's calculated from the maximum P_T trajectories. The overlap of these sets of ϕ_o's determines the momentum acceptance of this set of 8 fibers. After computing all 56 terms, we select the overall minimum and maximum value of P_T from the list. If the overlap is not zero, we have an equation and a P_T range for that equation. After checking all combinations of fibers from the original list in this manner, we have the complete set of equations involving the given innermost and anchor fibers. This operation is repeated for all fibers in the anchor layer in a sector of the CFT.

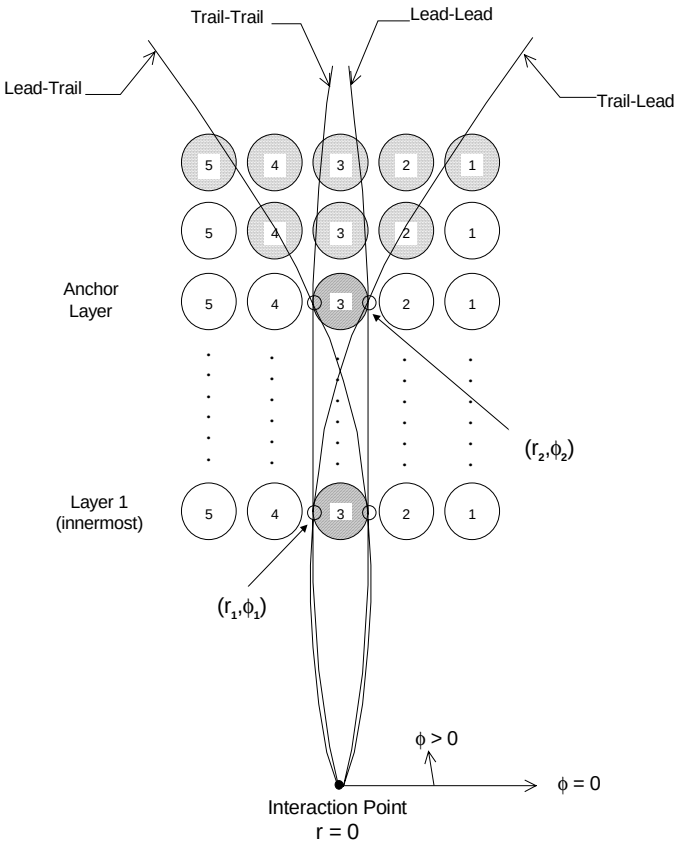

Figure 2: Track equation search region set by the boundary lines (lead-trail and trail-lead) defined by the edges of the reference fiber pairs on the innermost and anchor layers. The boundary lines are also the track with the maximum and minimum P_T that would intersect both the innermost and anchor fibers. The shaded fibers are those which are involved in the equation search.

The total number of analytically generated equations that require 8 out of 8 possible doublet layer hits is about 16000. After the experiment starts to run, we will be able to survey the CFT to obtain a physical set of track equations. Although we have assumed all tracks pass through the origin, the tracking efficiency for particles originated from points within 1 mm from the origin is still very good.

B. Track Pattern Recognition

The realization of these roads in the PLD's is conceptually very simple. The eight doublet layers of CFT are named as A, B, … H, from the innermost to the outermost. If a given

equation intersects A layer fiber bin 'a', B layer fiber bin 'b', and so forth out to H layer fiber bin 'h', then the equation can be programmed as an 8-fold logical AND in the PLD as:

$$\text{Trig}[a,b,...h] = \text{A}[a]\ \text{AND}\ \text{B}[b]\ \text{AND}\ ...\ \text{H}[h]. \quad (3)$$

The list of equations generated by the process described in the last section is actually a table of thousands of rows of doublet fiber bin numbers. The equations in the list are sorted or arranged according to certain P_T bins. On top of this list, we then use a text manipulation program to convert each row in this table into an equation formatted in VHDL (VHSIC Hardware Description Language), in order to be able to program the PLD's. These equations are of the following form:

$$\begin{aligned} \text{T1013172227323945} = \text{A}[10]\ \text{AND}\ \text{B}[13]\ \text{AND}\ \text{C}[17] \\ \text{AND}\ \text{D}[22]\ \text{AND}\ \text{E}[27]\ \text{AND}\ \text{F}[32] \\ \text{AND}\ \text{G}[39]\ \text{AND}\ \text{H}[45]; \end{aligned} \quad (4)$$

where the indices (10, 13, …,45) are the doublet bin numbers.

In the next step, the group of equations that share the same anchor layer (H layer in our baseline design) doublet bin, '45' in this case and belong to a chosen range of P_T (called 'pt15' in this example) are then logically OR'ed together:

$$\text{Trig\_pt15h45} = \text{T1013172227323945}\ \text{OR}\ \text{T}\ldots 45\ \text{OR}\ ... \quad (5)$$

Since the equations for a range of P_T are grouped together, each of these P_T groups is assigned a particular bit. The number of P_T groups in our baseline design is 16. As a result, the output from this stage is a matrix of pins which is 44 ϕ bin rows (since there are 44 fibers in the H layer of the CFT), by 16 P_T bin columns. Each pin in this matrix will be TRUE (1) if a track is found or FALSE (0) if no track is found.

It should be noted that there is the flexibility to vary the equation sorting criterion. In the baseline configuration, we sort the equations by their average P_T and we allow 16 P_T bins (corresponding to 16 P_T groups) though the track equations intrinsically have much finer resolution. We use 4 sets of PLD's to accommodate all the equations (about 16000). Since tracking algorithm and equation modifications during the experiment run is anticipated, we have to allow some flexibility in using these PLD's. Each unique fiber requires in principle one dedicated input (I/O pin in this case) to each PLD. Once the inputs are fixed, it is very difficult to change the inputs during the experiment run and this gives severe restrictions on what track equations may be put in each PLD's.

Without loss of generality, we apply the following 2 criteria to divide all the equations into 4 sets:

(i) 2 sets of H ϕ bins, namely, [1-22] and [23-44], i.e., two halves of a sector;

(ii) 2 momentum orientations in the radial plane of the CFT, positive and negative.

We lose no generality by using the above criteria because the number of fibers in the H layer is unlikely to change during the experiment run and there are always two opposite signs of momenta. Each set of equations is put into a set of PLD's which have all the fiber inputs needed by the equations for that particular set. In this way, each set of PLD's can accommodate track equations in the entire range of P_T. It turns out that the largest number of distinct fibers (or unique inputs to the PLD) that exist in each set is always less than 200, i.e., the number of input signals required for each PLD does not exceed 200. The input signals are multiplexed in 4 time slices in the FE board and therefore the number of inputs is only about 50. This allows us to use a PLD chip with a small number of inputs such as the moderately priced quad-flat-pack PLD.

C. Serialization of the Found Tracks

The track pattern recognition stage (in the above section) outputs a matrix of 22×16 pins in each set of the PLD's. The array must be searched in decreasing P_T order looking for any pins that are TRUE. As each TRUE pin is found, the ϕ bin address and P_T bin address for that pin are loaded into a register. This is basically a serial problem that must be solved in parallel hardware. If it were done serially the process would take at least $22 \times 16 = 352$ steps. To get a result every crossing this processor would have to make 352 steps times the 7.6 MHz crossing frequency which requires a clock rate of about 3 GHz. Alternatively the problem can be solved by applying PLD's utilizing a tree structure with many parallel branches in a very short time. However, this method requires significant resources. Most of the pins or elements in this matrix are FALSE since the occupancy of the 352 pins is expected to be less than 1%. Thus some shortcuts which are efficient in their use of logic resources can and have to be taken in solving the problem.

The serialization procedure in each PLD that we use is best described as follows:

(i) Each of the two-dimensional (22×16) bins is assigned an index number that codes its ϕ bin value (in H layer) and P_T bin value.

(ii) Further divide the equations of into a few subgroups of ϕ bins (such as a group of 5 or 6) and P_T bins (such as a group of 4) for parallel processing. Each parallel process is a "priority encoder" (described below) and is in serial mode.

(iii) For each of the ϕ bins, the 4 P_T bins are input into a priority encorder which outputs the indices of the 2 highest priority P_T bins that are TRUE[3] (i.e. there are candidate tracks in those ϕ-P_T bins). Information about any other bins that may have been TRUE are lost but this should happen less than ¼ % of the time.

(iv) The subgroups of indices are then regrouped into a one dimensional list of possibly 44 indices[4]. Each index is 5 bits (including sign) of P_T and those ϕ bins

[3] This is because we have to allow 2 tracks per ϕ bins as mentioned at the beginning of Section III.

[4] Equations in each PLD can have only 22 ϕ bins as we have grouped equations such that they have either ϕ bins [1-22] or [23-44] in the H layer.

which do not have candidate tracks would have indices equal to zeroes.

(v) The lists are concatenated in a binary tree structure down to a list of 6 and put into an output buffer.

The above steps are done in a mixed parallel/serial mode to reduce the latency for the process to its minimum as far as the resource allows us. In each PLD, there may have track equations with a range of P_T belonging two physics thresholds. An additional PLD needs to do a matching process from two sets of PLD's to fetch up to 6 tracks for each of the 4 P_T ranges as required and store the P_T and ϕ bits in a single buffer. Any information about any tracks beyond six is lost at the end of the above process.

D. Distribution of Triggers

After the tracking logic is completed, the tracking information is formatted. The number of tracks in 17 categories along with the beam crossing number and other diagnostic information are sent to the L1 trigger framework via a fast serial link for a final L1 decision. The information for a maximum of 6 tracks with the highest P_T is sent to the L1 muon trigger via another fast link. Up to 24 tracks are pipelined for later readout to the L2 trigger system. After leaving the CFT FE boards, all available CFT tracks are selected and combined into 6 global lists of up to 48 tracks each. These become the track seeds for the L2 trigger.

IV. TRIGGER SIMULATION

Monte Carlo simulation studies using the DØ upgrade configuration have been conducted on various physics samples. Single muon and electron samples are used to tune the efficiency of the algorithm code. Single and multiple interaction background samples are used to tune the fake track rejection of the algorithm. The baseline algorithm has an efficiency of more than 97% for the muon sample above 3 GeV and about 95% efficient for medium P_T electrons while maintaining good fake rejection. The efficiency is limited by multiple scattering which is more significant at lower P_T, and by radiation effects. More complicated physics samples such as top quark decays and $Z \rightarrow b\bar{b}$ have also been used in the Monte Carlo simulations to check that the baseline algorithm is indeed sound for various physics endeavors.

Different methods of sorting and ordering of the track equations in the PLD's can affect the tracking efficiency in the CFT. Here, we consider two ways of assigning a P_T bin. First, we can sort the equations by using the average P_T as in our baseline design. But, we can also use what is called the fiber "offset'' which is defined as follows. Imagine a track passing through fibers A_1 and H_1 on the innermost and anchor layers respectively. In the CFT radial plane, the straight line (corresponding to an infinite momentum track) drawn from the center of the detector to the center of the H_1 fiber would give an intersection fiber A_0 on the innermost layer. The "offset" is then (A_1-A_0) in the unit of fibers which is also an indicator of P_T. A larger offset implies a smaller P_T.

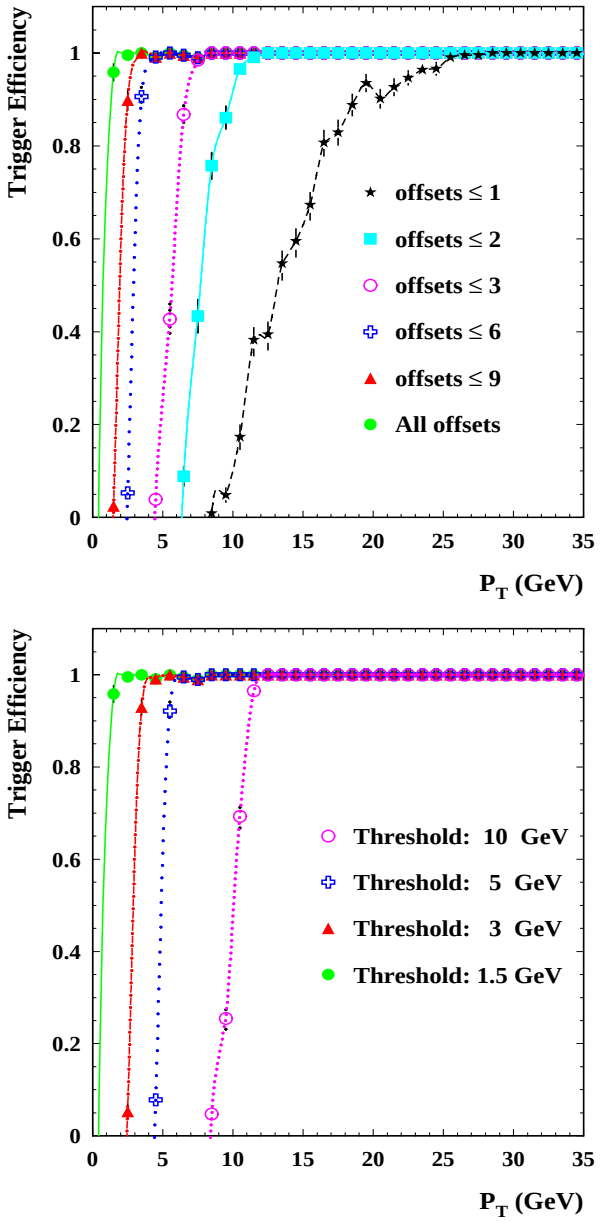

Figure 3: Top: CFT trigger efficiency vs momentum P_T turn-on curves when the fiber "offset" is used. Bottom: CFT trigger efficiency vs P_T turn-on curves when the average P_T of each equation is used. The latter is much sharper than the former.

In Figure 3, different CFT trigger efficiency curves due to different sortings and groupings of equations involved are shown versus P_T. The efficiencies would never jump abruptly from 0 to 100% due to the finite dimension of each scintillating fiber.

It is obvious in Figure 3 that the efficiency versus P_T turn-on (rising from 0 to almost full efficiency) at about 10 GeV is significantly different depending on whether we use the fiber offset or the average P_T of each equation. The turn-on curve is significantly sharper in the latter case. This is because the intrinsic resolution in each equation is better than that of a fiber. These plots also illustrate how the fiber offset varies with the P_T. Therefore, using the average P_T of the equation is superior to using the fiber offset in the trigger algorithm.

V. SUMMARY

A fast deadtime-less L1 trigger system has been developed for the DØ Central Fiber Tracker (CFT). The CFT trigger system consists of Visible Light Photon Counters, sophisticated digitization and discrimination electronics plus fast pipelined trigger logic which is based upon the use of large PLD's. The trigger logic for the PLD's has been simulated and verified using a dedicated trigger test board.

Monte Carlo simulation has been done along with the hardware design to make sure that the design meets for all envisioned physics requirements, and to fine-tune the efficiency of the tracking algorithm.

VI. REFERENCES

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